REMARKS

In an office action dated November 4, 2003, the Examiner objected to the title as non-descriptive, and rejected claims 1-14 under 35 U.S.C. 102(b) as being anticipated by Janik et al. (U.S. Patent 6,163,839).

Title

The Examiner objected to the title, but did not suggest any particular amendment to the title or feature that should be mentioned in the title. Applicants have amended the title in a manner believed to make it more descriptive of the claimed invention, and to satisfy the Examiner's objection. If the Examiner is of the opinion that, notwithstanding the amendment, the title is still insufficiently descriptive, applicants respectfully request that the Examiner suggest some language or feature that should be included in the title.

Prior Art

Applicants have amended independent claims 1 and 8 to more specifically recite significant features of the claimed invention. In particular, the independent claims are amended to clarify that data tags pass through the successive stages of the pipeline in unison with the data with which they are associated, i.e., a data tag is always in the same pipeline stage as the data with which it is associated; and that data tags are matched with control tags to control the passage of data and tags from one stage to the next. As amended, the claims are patentable over the cited art.

Applicants' invention relates to stage control in an asynchronous pipeline. In a conventional synchronous pipeline, data advances from one stage to the next responsive to a clock signal, which is generally derived from a global processor clock. It is therefore relatively easy to predict the progress of data through the pipeline at any given time. An

asynchronous pipeline does not use a global clock, and generally uses internal logic which determines when some particular data set is ready to advance to the next pipeline stage. The asynchronous pipeline is thus potentially faster, since it doesn't need to wait for the worst case stage delay, but the variable delay makes it more difficult to predict data progress through the pipeline.

In accordance with applicants' invention, a data tag is associated with each data set processed by the pipeline, the tag moving through the pipeline in unison with the associated data set. Advancing from one stage to the next is controlled by internal logic which uses, among other factors, a comparison of the data tag with a control tag. The data set and its tag are allowed to advance to the next pipeline stage only if the data tag matches the control tag. Typically, some other condition or conditions, which may be conventional, must be met in addition to matching the data tag with the control tag. Use of the data tag and control tag to control advancing through the pipeline permit external logic to control the asynchronous pipeline, so that, e.g., data sets may be halted at some arbitrary stage pending some other action, timed according to some external timing conditions, etc.

Janik discloses a synchronous "counterflow" pipeline architecture for a processor, in which an instruction pipeline is arranged in physical proximity to a result pipeline, the two flowing in parallel and in opposite directions. Stages in the instruction pipeline correspond to stages in the result pipeline in reverse order, allowing results of recent operations to be transferred to the instruction pipeline where needed in a subsequent operation. When ready to execute, an instruction is dispatched to an execution unit. Results from the execution are placed in the result pipeline in the first available slot. A tag is associated with instructions and results, by which it is possible to match results with the instructions which produced them. This is necessary because results are not always produced in sequence.

Although *Janik* discloses pipelines and tags associated with data in a pipeline, *Janik*'s tags perform an essentially different function from those performed by applicants' tags, and *Janik*'s pipeline architecture is substantially different. Applicants' pipeline is an asynchronous pipeline, in which the logic conditions which govern the passage of data from one stage to the next include matching the data tag accompanying the data with a control tag associated with the next pipeline stage. In this manner, the stage at which data resides at any given time can be subject to external control. *Janik*'s pipeline is synchronous (controlled by a clock), although asynchronous pipeline operation is mentioned in the patent. But more importantly, *Janik*'s tags do not control the passage of data from one stage to another. They are used to identify the instruction which produced data, for purposes of multi-threading and data coherency.

Applicants' representative amended claim 1 recites:

> 1. A method for externally managing data within an asynchronous pipeline, wherein said asynchronous pipeline includes a plurality of pipeline stages, and a data path and a control path traversing said plurality of pipeline stages in unison, said method comprising:
>
> assigning a respective data tag value to each of a plurality of data sets, each said data set for input to said asynchronous pipeline in a respective input interval;
>
> sending each said respective data tag value into said control path when said data set to which the respective data tag value is assigned is sent into said data path such that said respective data tag value passes through each successive stage of said plurality of stages of said asynchronous pipeline in unison with said data set to which the respective data tag value is assigned; and
>
> comparing each said data tag value with a respective control tag value associated with a given stage of said asynchronous pipeline; and
>
> *in response to a data tag value matching a respective control tag value, permitting said matching data tag value and the data set to which said matching data tag value is assigned to pass in unison to a next stage* within said asynchronous pipeline. {emphasis added]

Independent claim 8, although not identical in scope, contains limitations analogous to the italicized language.

Because *Janik*'s tags are used only to match data with the instructions which produced them, and not to control the passage of data from one pipeline stage to the next, claims 1 and 8, as amended, are not anticipated by *Janik*.

Nor are the amended independent claims obvious over *Janik*. Although *Janik* discloses asynchronous pipelines in its background, and suggests the use of asynchronous pipelines in the general sense, there is no specific disclosure of how the passage of data from one successive pipeline stage to the next would be asynchronously controlled. At most, *Janik* suggests that a pipeline apparatus similar to that disclosed in the patent could be controlled asynchronously using conventional means, as opposed to control be a clock as in the preferred embodiment. There is no suggestion that the tags which are used to identify the instructions producing data should be used for controlling the pipeline operation, i.e., the passage of data from one successive pipeline stage to the next, as recited in applicants' claims. Accordingly, any suggestion to modify the operation of *Janik*'s tags in some way as to come within the scope of the claims is absent, and the claims as amended are not obvious over *Janik*..

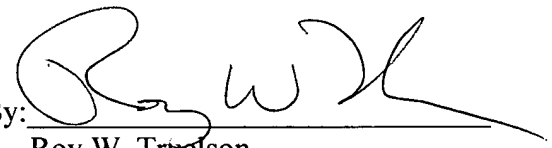
New claim 15 recites an asynchronous pipeline, having "stage advance control logic which controls the advancing of each data set and its corresponding tag through successive ... ordered stages" upon the satisfaction of respective logical conditions, where at least some stages include the condition that the data tag match the control tag. Although this limitation is not identical in scope with those described above with respect to claim 1, it is similarly not disclosed or suggested by *Janik* for essentially the reasons explained above.

In view of the foregoing, applicants submit that the claims are now in condition for allowance and respectfully request reconsideration and allowance of all claims. In

addition, the Examiner is encouraged to contact applicants' attorney by telephone if there are outstanding issues left to be resolved to place this case in condition for allowance.

Respectfully submitted,

PETER W. COOK, et al.

By: 

Roy W. Truelson
Registration No. 34,265

Telephone: (507) 289-6256